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Design and analysis of single layer quantum dot-cellular automata based 1- bit comparators

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ABSTRACT

Quantum dot-cellular automata (QCA) technology has recently emerged as a potential candidate for the design of nanometer-scale computational circuits. In digital logic circuits, the comparator is the basic building block for comparing two binary values. This paper presents and implements two 1-bit QCA-based comparator designs. The proposed QCA implementations are compact, require only a single layer and are less complex compared to recently reported designs. The QCADesigner tool has been used to confirm the functional validity of the proposed QCA structures. The simulation results of the proposed comparators have shown considerable improvements compared to their existing counterparts in terms of the number of QCA cells and occupational area requirements in addition to cost and efficient complexity values. Furthermore, all of the proposed structures are dissipating extremely low energy values. Thus, the proposed QCA-based comparators can be viewed as viable options for low power digital applications.

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1. INTRODUCTION

Complementary metal oxide semiconductor (CMOS) scaling has been the key driving force behind the development of higher density and faster computing systems in the microelectronics industry [1]. In the last few decades, according to Moore's law, the number of transistors per chip and the performance of the digital systems have increased exponentially. However, the increasing density of transistors per chip has caused an increased dissipation of power in the digital system. More integration levels and improved device performance have also increased the propensity to scale almost all of the parameters within the device structure such as effective channel length, gate oxide thickness, and junction depths. Some of these parameters have, however, reached their physical limits [1]-[4]. As a result, alternatives to current materials and device structures need to be found in order to pursue device scaling. One of the promising alternative technologies is Quantum dot-cellular automata (QCA) technology, which can be considered as a potential candidate for overcoming the physical difficulties in the existing CMOS technology due to its unique features including high switching speed, improved packing density and reduced energy dissipation [3], [5]. In QCA technology, the basic cell consists of four quantum dots containing two electrons capable of tunneling between adjacent dots. The position of the electrons represents the logical state of the cell [4], [6]. Unlike traditional CMOS structures in which the information is transmitted via the flow of electrical current, the QCA technology relies on the columbic interactions among adjacent cells to enable data transmission [4].

Various strategies for data transmission and computation are usually used to build logical circuits on the basis of a nano-scale QCA technology [4], [7]. However, as the QCA technology utilizes electrostatic repulsions to propagate the logic data, there is no existing guarantee that the information will move to the desired direction. To ensure proper data flow in QCA-based designs, QCA circuit clocking mechanisms are introduced [8]. In fact, designs based on QCA technology are clocked in four sequential phases including the switch, hold, release and relax. The electric field caused by the clock signal is used to increase or decrease the tunneling barrier of quantum dots in the QCA cell. The electrons can be transferred from one dot to another inside the QCA cell when the potential of the tunneling barrier is low. However, if the potential barrier is strong, the electrons are locked within the dots and the external electrical fields have little impact on the state of the cell. In order to steer the transmission of information across adjacent cells in a QCA-based structure, four clocking zones are typically used with each clocking zone shifted by 90° with respect to its preceeding clock zone [9], [10].

In QCA technology, the inverter and the majority gate are the two basic building blocks used to achieve more logical functionality. The AND and OR operations can be performed by either setting the '0' logic or the '1' logic to a specific input of the majority gate [4], [8], [11]. In order to allow a certain degree of design versatility in QCA technology, two types of wiring crossovers are usually used, namely, coplanar and multilayer crossover techniques. The coplanar crossing uses only one layer and uses both 45° and 90° cells so that they do not interfere with each other. However, the coplanar crossover has low immunity against structural defects and can fail during the processing of QCA-based structures [4], [7], [11]. On the other hand, multi-layer crossover uses a peculiar number of layers, usually three layers. The entire circuit is mainly constructed on the bottom layer while the crossover wires are located on the top and the middle layers to serve as a connection between the layers. Compared to coplanar based structures, the multilayer crossover consumes less area despite the increased manufacturing complexity [7].

In recent years, extensive research works have proposed many computational and storage QCA-based circuits such as arithmetic and logic unit (ALU) [12]-[14], counters [15]-[17], multipliers [18], [19], nano-sensor data processors [20] and adders and substractors [21]-[23]. Evidently, the diversity of QCA-based logic and memory structures is introducing QCA technology as an important candidate for future computing systems. In this context, the comparator is a critical component in a plethora of digital applications including processors, microcontrollers and digital communication systems [24]-[26]. It has the function of defining three states of two n-bit numbers, which may be provided in serial or parallel manner, and then comparing and providing three possible cases: equal, larger, or smaller than each other [24]-[27]. The authors of [28] have introduced QCA implementation of a single-bit comparator using reversible Feynman QCA gates. Their proposed structure consists of 87 cells and occupies an area of 0.11 μm^2. In their study, three Feynman QCA gates were used to achieve the intended outputs (A>B, A<B and A=B). Roy *et al*. [25] have proposed two implementations of 1-bit comparator using the layered-T AND and OR gates. The number of cells requirement of their proposed designs was 40 and 37 QCA cells with an occupational area of 0.032 μm^2 and 0.028 μm^2, respectively. Moreover, Umira *et al*. [27] have proposed a 1-bit comparator using a universal gate. Their proposed comparator uses 58 QCA cell with an occupational area of 0.055 μm^2 and a latency of 3 clock cycles. In addition, the authors of [29] have implemented a multilayer QCA-based comparator using a five-input majority gate. In their research work, a 1-bit comparator with a delay of three clock cycles has been presented. Nevertheless, the proposed comparators are not achieving significant improvements in the number of QCA cells and area requirements. Deng *et al*. [30] have introduced an XNOR gate-based implementation of multi-bit comparators. In their paper, a reliable and efficient XNOR QCA-based structure was firstly proposed. Thereafter, the authors have used the proposed XNOR to implement multi-bit comparator circuits. Their proposed comparators are multilayer and have achieved less complexity values. Recently, a coplanar 1-bit QCA comparator structure has been presented in [31]. Their proposed coplanar QCA comparator was built on the basis of the fundamental QCA logic gates including the majority, XNOR and inverter gates. Their implemented QCA-based comparator reduces cell count, occupied area, latency and cost with respect to earlier existing structures. More recently, Gao *et al*. [26] have proposed a 1-bit QCA comparator utitlizing a single layer and 31 QCA cells with an occupational area of 0.04 μm^2. Their proposed structure has required two AND gates, one OR gate and three inverters. In fact, there is a considerable attention to the implementation of high-performance, area- and energy-efficient comparator circuits. Therefore, recent attempts have been made to improve the performance of comparator circuits which remain widely investigated and optimized [26], [30], [31]. In this paper, area-efficient comparator structures are designed and implemented based on QCA technology. The evaluation of the functionality of the proposed circuits is carried out a specialized QCA design tool. Comprehensive comparisons have been made between the proposed comparators and the recently published designs. Evaluation results show that the presented designs have greatly reduced cell count, area requirements when compared with the best recently reported designs.

The remainder of this paper is structured as follows: section 2 introduces the proposed 1-bit comparator structures. Section 3 explores the functional validity of the proposed designs, evaluates their performance, estimates their energy dissipation and compares them to their recently reported designs. The conclusions are eventually drawn in section 4.

2. PROPOSED COMPARATOR STRUCTURES

Two area-efficient 1-bit comparator designs based on the QCA technology are successively presented in this section. Figures 1 and 2 show the proposed single-layer 1-bit comparators. As shown, the comparator circuit compares the two binary inputs labelled as A and B and and generates three output signals, namely: $F_{A=B}$, $F_{A>B}$ and $F_{A<B}$ following the logic functionality shown in Table 1. The algebraic expressions describing the behavior of 1-bit comparator are given in (1).

$$\begin{aligned} F_{A=B} &= \overline{A \oplus B} \\ F_{A>B} &= A \,.\, \overline{B} \\ F_{A<B} &= \overline{A} \,.\, B \end{aligned} \tag{1}$$

Table 1. One-bit comparator truth table

A	B	$F_{A=B}$	$F_{A>B}$	$F_{A<B}$
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

The first proposed single layer 1-bit comparator (Design A) is illustrated in Figure 1. As shown, the proposed structure is implemented using 3-clock zones to influence the direction of the data flow and also to propagate the computational results to the output cells. The proposed structure includes two 3-input majority gates to obtain outputs ($F_{A>B}$) and ($F_{A<B}$). The output ($F_{A=B}$) is then generated by feeding the other two outputs (i.e., ($F_{A>B}$) and ($F_{A<B}$)) to an additional majority gate. The proposed 1-bit comparator design uses only 23 cells without the need for any wiring crossover. Moreover, it can be noticed that the outputs ($F_{A>B}$) and ($F_{A<B}$) are accomplished using two clock zones (i.e. clock zone 0 and 1) while the output ($F_{A=B}$) is produced using three clock zones (i.e. clock zone 0, 1 and 2).

The second proposed 1-bit single-layer comparator circuit (Design B) is depcited in Figure 2. The proposed 1-bit comparator is compact and requires only 14 QCA cells with an area of 0.02 μm^2. In addition, it does not require any type of crossover. In this design, the outputs ($F_{A<B}$, $F_{A>B}$ and $F_{A=B}$) are obtained by utilizing two clock zones (i.e. clock zone 0 and 1). The achieved improvement of the second proposed design as compared to the first one in terms of cell count is found to be 64.3%. Furthermore, the second proposed structure has lower output delay as it is clocked using two clock zones.

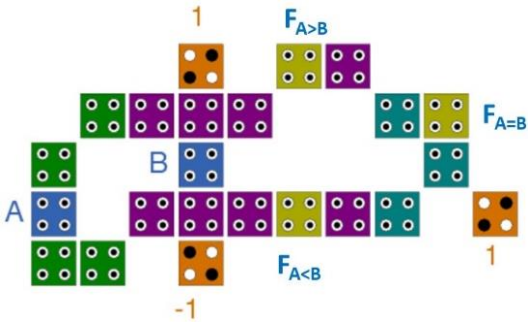

Figure 1. The first proposed structure - Design A

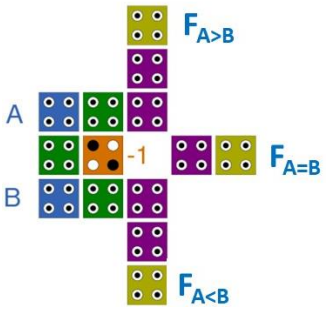

Figure 2. The second proposed structure - Design B

3. RESULTS AND DISCUSSIONS

The QCADesigner-ver-2.0.3 simulation tool [32] was employed to evaluate the functionality of proposed 1-bit comparator structures and also to determine their structural costs (i.e., number of cells, area and output delay). In this study, the simulation parameters are configured as shown in Table 2. Figure 3 shows the

simulation results of the first proposed structure (Design A). As shown, the results prove the functional validity of the proposed structure as compared with the logical values shown in Table 1. As can be seen from Figure 3, when the input (A) is equal to input (B), only the corresponding output ($F_{A=B}$) will be activated. On the other hand, if the input (A) is greater than the input (B), only the output labeled as ($F_{A>B}$) will be asserted. Alternatively, the output labeled as ($F_{A<B}$) is activated once the input (A) is lower than the input (B). Moreover, it can be noticed that the outputs ($F_{A>B}$) and ($F_{A<B}$) are delayed by 0.5 clock cycle from the inputs, while the output ($F_{A=B}$) is delayed by 0.75 clock cycle.

Table 2. Simulation configuration

Parameter	Value
QCA cell width	18 nm
Cell height	18 nm
Diameter of the quantum dot	5 nm
Number of samples	12800
Number of iterations per sample	10000
Radius of effect	65 nm
Layer separation	11.5 nm

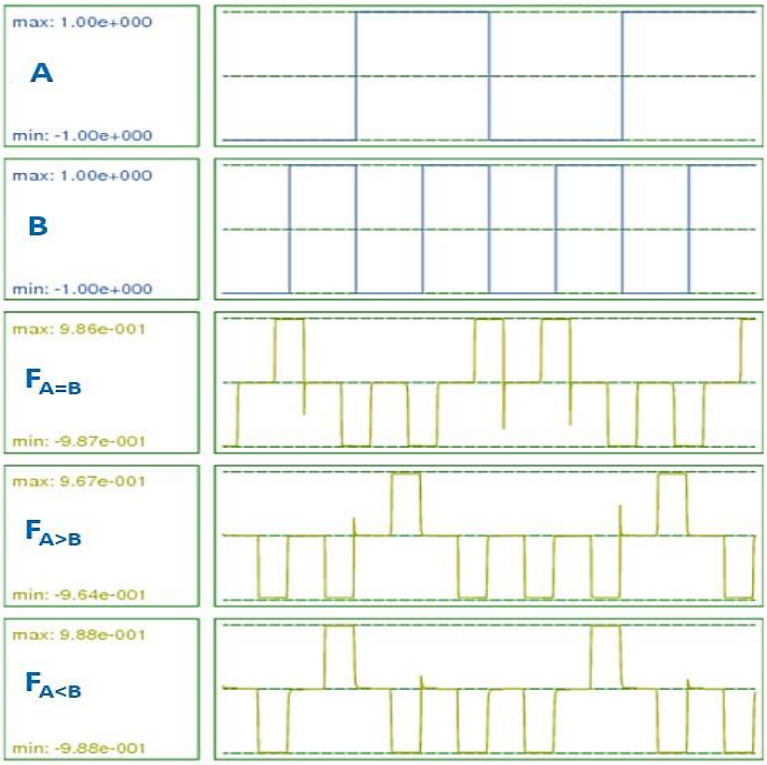

Figure 3. Simulation results of the first proposed 1-bit comparator-Design A

The simulation results for the second proposed 1-bit comparator (Design B) is shown in Figure 4. Apparently, the proposed design achieves the intended comparison functionality. In addition, all of the outputs in this structure are obtained after a delay of 0.5 clock cycle after the application of input signals. Hence, the second proposed structure is 33% faster than its first counterpart. Additionally, Figure 5 compares the proposed structures in terms of cell count (i.e., structural complexity) and occupational area. As depcied, the second proposed structure (Design B) significantly reduces the number of QCA cells and occupational area requrements as compared with Design A. The achieved reductions in cell count and occupational area have reached 39% and 33%, respectively.

Moreover, the QCADesigner-E tool [33] has been utilized to compute the energy dissipation of the proposed structures. Figure 6 presents the total and average energy dissipations of the proposed structures. As shown, both of the proposed designs have low total and average energy dissipation levels. As compared to the first proposed design (Design A), the second proposed design (Design B) has lower total and average energy

dissipation values. The achieved improvements in total and average energy dissipations have been found to be 30.5% and 30.55% respectively.

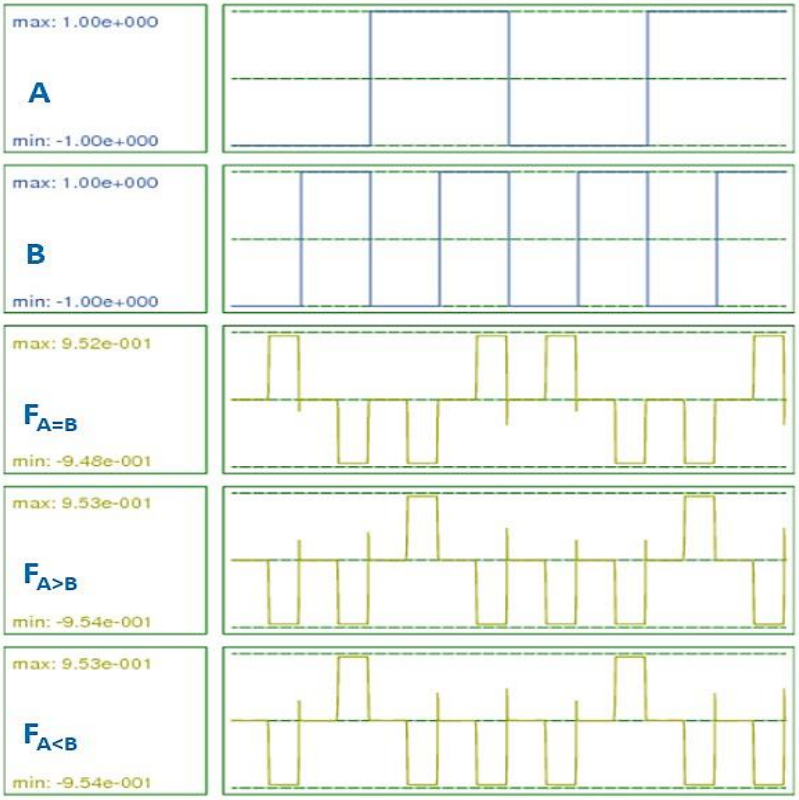

Figure 4. Simulation results of the second proposed 1-bit comparator-Design B

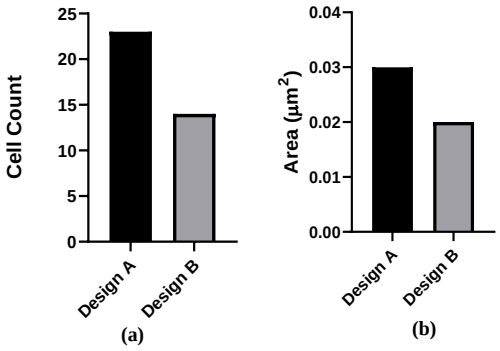

Figure 5. Comparisons of (a) cell count and (b) area of the proposed comparator structures

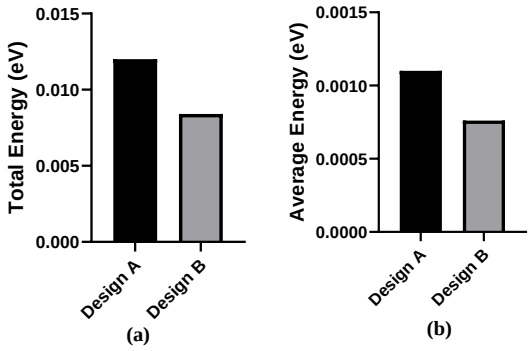

Figure 6. Comparisons of (a) total energy and (b) average energy dissipations of the proposed comparator structures

Moreover, key comparison factors in designing and evaluating QCA-based structures are cost and efficient complexity factors. In fact, the cost value depends on the area of QCA structure in μm^2 and the output delay per clock cycle as given in (2) [31], [34].

$$Cost = Area.Delay^2 \quad (2)$$

On the other hand, the efficient complexity (EC) is determined using formula given in (3) [30].

$$Efficient\ Complexity = Cell\ count.Area^{1/n} \quad (3)$$

where n is the number of QCA layers.

Figure 7 shows comparison of the proposed designs in terms of cost and efficient complexity values. As shown, the second proposed design (Design B) has lower cost and efficient complexity values when compared with its first counterpart. The achieved reductions in both values have reached approximitly 70%. Table 3 summarizes and compares the proposed structures with other existing QCA-based comparators.

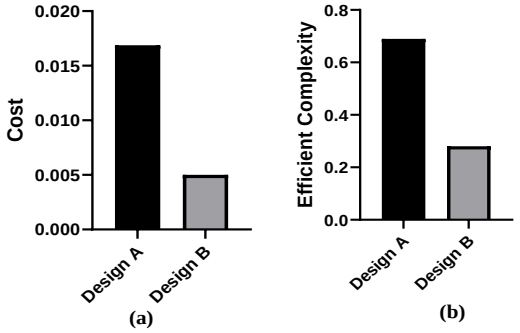

Figure 7. Comparisons of (a) cost and (b) efficient complexity values for the proposed comparator structures

Table 3. Comparisons between the proposed comparators and recent designs

Reference	Cell count	Area (μm^2)	Time delay (clock cycle)	Crossover	Cost	Efficient Complexity
[28]	87	0.11	0.5	Coplanar	0.0275	9.57
[31]	38	0.03	0.5	Coplanar	0.0075	1.14
[30]	42	0.05	0.75	Not required	0.0281	2.1
[25]	37	0.028	1	Multilayer	0.028	11.2
[27]	58	0.055	0.75	Not required	0.031	3.19
[29]	100	0.11	0.75	Multilayer	0.0618	47.9
[26]	31	0.04	0.75	Not required	0.0225	1.24
Design A	23	0.03	0.75	Not required	0.0169	0.69
Design B	14	0.02	0.5	Not required	0.005	0.28

The comparison parameters are cell count, area, delay, crossover type, cost and efficient complexity (EC) values. As shown, the proposed 1-bit comparator structures (Design A and B) outperform the recently reported designs. In addition, the proposed designs have achieved a reduction of 25.8% and 54.5% respectively in the number of cell requirements relative to the most recent structure proposed in [26]. Moreover, the proposed QCA-based structures require less occupational area as compared with the best reported design [26]. The achieved reduction in the efficient complexity (EC) value has reached up to 26% with respect to that of [26]. In addition, as compared to the first proposed structure (Design A), the area occupied of the design presented in [25] is smaller. However, this reduction in area was due to the increased number of QCA layers (i.e., multilayers) and not primarily from the logic design. This is directly reflected in the high value of efficient complexity (EC) of such structure. Moreover, in contrast to the first proposed design (Design A), the structure proposed in [31] has a similar occupational area. However, this is based on a coplanar crossover that is susceptible to failure and may have major issues with reliability during manufacturing of such type of QCA- based circuits [4], [7], [11]. Furthermore, the second proposed design (Design B) outperforms all recent reported designs in terms of the number of QCA cells and area requirements. The achieved reductions in cell count and area have reached up to 54.5% and 75% respectively when compared to the most recent comparator design in [26]. The cost and efficient complexity (EC) values have been reduced by 78% and 77.4% relative to that of [26]. Finally, the proposed structures provide alternative 1-bit QCA-based comparator designs with efficient occupational area, cell count without the need for multilayer and coplanar crossover wiring techniques.

4. CONCLUSION

In this article, two different 1-bit comparator QCA-based structures were introduced and thoroughly evaluated. The logical correctness of the proposed comparators has been verified using the QCADesigner tool. In addition, the energy dissipation values have been estimated using the QCADesigner-E tool. Performance

comparisons with the previously reported designs in terms of key design factors such as area, cell count, delay, cost, and efficient complexity values were also included. The proposed 1-bit comparator structures (Design A and B) have achieved 25.8 % and 54.5% reductions in the number of cell requirements when compared to the most recent comparator design. In addition, the obtained reductions in efficient have reached up to 44.3% and 77.4% as compared with the best existing design. In future, the proposed QCA designs can be expanded to n-bit comparators so that many arithmetic circuits are efficiently constructed.

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